In the Claims:

Please amend the claims as follows:

1. (Canceled)

2. (Previously Presented) The memory according to claim 3, in which said array configuration circuit includes, for each sub-array of memory elements, an input selector associated with a first memory element of the sub-array, for selectively feeding the first memory element with either an output of a last memory element in an adjacent previous sub-array, in the first operating configuration, or an output of a last memory element of the sub-array, in the second operating configuration.

3. (Currently amended) A memory comprising:

at least one array of memory elements;

a partition of the at least one array into a plurality of sub-arrays of the memory elements;

an array configuration circuit for selectively ~~putting~~ placing the at least one array in one of two operating configurations, the two operating configurations including:

a first operating configuration, in which the memory elements of the at least one array are coupled one to another to form a monodimensional sequentially-accessible memory, and

a second operating configuration, in which the memory elements in each sub-array are coupled to one another so as to form an independent monodimensional sequentially-accessible memory block, the memory blocks of each sub-array being isolated from the memory blocks of the other sub-arrays, and a data

content of any memory element of the sub-array being rotatable by shifts through the memory elements of the sub-array;

a sub-array selector, responsive to a first memory address, for selecting one among the plurality of sub-arrays according to the first memory address, the sub-array selector enabling access to the selected sub-array;

a memory element access circuit, responsive to a second memory address, for enabling access to a prescribed memory element in the selected sub-array after a prescribed number of shifts, depending on the second memory address, of the data content of the memory elements in the selected sub-array;

wherein the first operating configuration is a data storage configuration in which the memory is ~~put~~placed when data are to be stored therein; and

wherein the second operating configuration is a data retrieval configuration in which the memory is ~~put~~placed when data are to be retrieved therefrom.

4. (Previously Presented) The memory according to claim 3, in which in the second operating configuration each sub-array provides a respective output data, the sub-array selector selecting one sub-array output data out of the output data provided by the plurality of sub-arrays, according to the first address.

5. (Original) The memory according to claim 4, in which said memory element access circuit enables a transfer of the output data of the selected sub-array to a memory output after a prescribed number of shifts of the data content of the memory elements in the selected sub-array.

6. (Original) The memory according to claim 5, in which said memory element access circuit includes a counter for counting the number of data content shifts, and a coincidence detector detecting coincidence between a counter

value and a value representative of the second address, the coincidence detector enabling the transfer of the output data of the selected sub-array to the memory output when the counter value equals the value representative of the second address.

7. (Previously Presented) The memory according to claim 3, in which each memory element includes at least one flip-flop.

8. (Currently Amended) A memory, comprising:

a plurality of memory locations; and

a control circuit coupled to the memory ~~locations~~ and operable to,

~~allow~~ provide random access to the memory locations ~~during~~ responsive to a read ~~mode of~~ operation, and

~~allow~~ provide sequential access to the memory locations ~~during~~ responsive to a write ~~mode of~~ operation.

9. (Currently Amended) The memory of claim 8 wherein the control circuit ~~allows~~ provides sequential access to the memory locations during the write ~~mode of~~ operation so that the memory functions as a first-in-first-out memory.

10. (Canceled)

11. (Canceled)

12. (Currently amended) A memory, comprising:

an array of memory locations; and

a control circuit coupled to the array and operable to cause the array to operate as

a random-access memory during ~~a~~ all read ~~mode of operation~~ operations, and

a first-in-first-out memory during ~~a~~ all write ~~mode of operation~~ operations, wherein:

the memory locations comprise rings of serially coupled memory locations each having a respective contents, with the contents of each ring being independent of the contents of the other rings; and

during the first mode of operation, the control circuit is operable to control each of the rings to,

receive a clock signal,

shift the contents of each respective memory location in the ring to a respective next memory location in the ring once per cycle of the clock signal, and

allow access to one of the memory locations during a predetermined cycle of the clock signal.

13. (Previously Presented) The memory of claim 12 wherein:

the memory locations comprise a ring of a number *n* of serially coupled memory locations each having a respective contents; and

during the read mode of operation, the control circuit is operable to,

receive a clock signal,

shift the contents of each respective memory location in the ring to a respective next memory location in the ring once per cycle of the clock signal for *n* clock cycles, and

allow access to a predetermined one of the memory locations during a predetermined cycle of the clock signal.

14. (Currently amended) An electronic system, comprising:

a memory, comprising,

a plurality of memory locations, and

a control circuit coupled to the memory locations and operable to,

~~allow~~ force random access to the memory locations ~~during~~ responsive to a read ~~mode of~~ operation, and

~~allow~~ force sequential access to the contents of the memory locations via one of the memory locations ~~during~~ responsive to a write ~~mode of~~ operation.

15. (Previously Presented) A method, comprising:

randomly accessing memory locations of a memory during either a read mode or a write mode of operation, and

sequentially accessing the memory locations via one of the memory locations during the read or write mode of operation, wherein the sequential accessing occurs during the alternate mode of operation as does the randomly accessing.

16. (Original) The method of claim 15 wherein randomly accessing the memory locations comprises:

accessing a first memory location having a first address; and

accessing a second memory location having a second address.

17. (Original) The method of claim 15 wherein sequentially accessing the memory locations comprises:

reading first data from a first memory location;

shifting second data from a second memory location into the first memory location; and

reading the second data from the first memory location.

18. (Original) The method of claim 15 wherein sequentially accessing the memory locations comprises:

writing first data to a first memory location;

shifting the first data from the first memory location to a second memory location; and

writing second data to the first memory location.

19. (Original) The method of claim 15 wherein randomly accessing the memory locations comprises:

shifting the contents of each respective memory location to a respective next memory location a number of times; and

accessing a predetermined one of the memory locations after a predetermined one of the shifts.

20. (Original) The method of claim 15 wherein randomly accessing the memory locations comprises:

shifting the contents of each of *n* respective memory locations to a respective next one of the *n* memory locations *n* times; and

accessing a predetermined one of the *n* memory locations after a predetermined one of the *n* shifts.